

Attorney Docket No.: CPAC 1017-5  
Application No. 10/632,552

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**Remarks**

Claim 1 is amended to correct a typographical error ("such a" is replaced with -- such that a --) Claims 20 - 34 are canceled herein without disclaimer or prejudice to Applicant's right to prosecute claims to the subject matter therein by way of one or more continuing applications.

Claims 1 - 17, 19, 35 and 36 are now in the application.

Reconsideration of the application as amended is requested.

The points raised by the Examiner will now be addressed, beginning with the rejections under 35 U.S.C. § 102.

**Rejections under 35 U.S.C. § 102**

Claims 1 - 4, 11, 12, 17, 35 and 36 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kikuma *et al.* U.S. 6,621,169 ("Kikuma"). The Examiner characterized Kikuma as follows:

Regarding claim 1, Kikuma et al. discloses in Fig. 9A a multi-package module (50) comprising:

- first (32-2 and 52-2) and second (32-3, 52-3 and 52-4) packages,
- each said package including a die (52-4 and 52-2) attached to a passive substrate (32-3 and 32-2),
- each said substrate having a die attach side and a land side (see e.g., Fig. 9A),
- wherein the second package (32-3, 52-3 and 52-4) is stacked over the first package (32-2 and 52-2) such a portion of the land side of the second package (32-3) opposite the second package die is affixed (thru the element 52-3) to a surface of the first package (32-2 and 52-2),
- wherein the first (32-2) and second (32-3) substrates are interconnected by wire bonding (the wire; see e.g., Fig. 9A), and wherein the first package (32-2 and 52-2) comprises a flip-chip ball grid array package having a flip-chip (52-2) in a die-up configuration (see e.g., Fig. 9A).

Applicant, respectfully, disagrees with the Examiner's reading of Kikuma and application of it to Applicant's invention. As explained below, Kikuma does not teach or suggest a multi-package module including stacked packages, as in Applicant's claimed invention (nor does

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Kikuma teach or suggest a method for making a multi-package module, by providing first and second packages, at least one of which is a stacked die package, stacking one package over the other, and electrically interconnecting the packages by wire bonding).

The Examiner identifies features (32-2 and 52-2) as a "first package" comprising a "flip-chip ball grid array package" in Kikuma. Applicant disagrees with this characterization. Features 32-2 and 52-2 do not constitute a ball grid array package. There is no second-level solder ball array on substrate 32-2. (A flexible printed wiring board (first substrate) 26 is shown with solder balls in Kikuma Fig. 9A (see also Fig. 10), but it is not a part of a flip-chip ball grid array package.)

The Examiner identifies features (32-3, 52-3 and 52-4) as a "second package" in Kikuma, and refers generally to Fig. 9A as showing each substrate having a land side and a die attach side. Then the Examiner asserts that "the second package (32-3, 52-3 and 52-4) is stacked over the first package (32-2 and 52-2) such a portion of the land side of the second package substrate (32-3) opposite the second package die is affixed (thru the element 52-3) to a surface of the first package (32-2 and 52-2)". The Examiner appears to take the position that the downward-facing side of the substrate 32-3 is the "land side" (accordingly the upward-facing side of the substrate 32-3 is the "die attach side" of the substrate, and the die 52-4 is the die attached thereto), inasmuch as he states that "a portion of" the said "land side" of the second package (32-3, 52-3 and 52-4) "is affixed (thru the element 52-3) to a surface of the first package. But the feature 52-3 is a die and the Examiner does not appear to take the position that the die 52-3 is a part of a first package. Accordingly, the **second substrate is not affixed to a surface of the first substrate.**

Kikuma describes a "stacked semiconductor device" having "a plurality of semiconductor chips of desired sizes stacked as one package". The Kikuma device of Fig. 3, for example, is constructed (see, Figs. 4A - 4F; Col. 8, line 39 - Col. 9, line 10) as follows. A first semiconductor chip 22 is mounted onto a printed circuit board 32 by flip-chip bonding (Fig. 4B). Then the reverse face of the semiconductor chip 22 is attached using an adhesive to a surface of a flexible printed wiring board 26, and a second semiconductor chip 24 is attached using an adhesive to a surface of the printed circuit board 32 (Fig. 4C). Then the printed circuit board 32 is electrically connected to the printed wiring board 26 by bonding wires (effecting electrical connection of the

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first semiconductor chip 22 to the printed wiring board 26 by way of the printed circuit board); and the second semiconductor chip 24 is electrically connected -- also to the printed wiring board -- by bonding wires (Fig. 4D). Then "the semiconductor chips and their bonding wires" are encapsulated by an encapsulating resin 40 (Fig. 4E), and solder balls 30 are mounted on the printed wiring board to complete the device (Fig. 4F).

The Kikuma device of Figs. 9A, 9B is constructed in the same way (see, Col. 11, lines 15 - 63). These Figs. "show examples in each of which a plurality of semiconductor chips are stacked in accordance with the first embodiment of the present invention." (Col. 11, lines 15 - 17.) In the examples of both Fig. 9A and 9B "four semiconductor chips of the same types are stacked, and second substrates are interposed between the semiconductor chips." (Col. 11, lines 17 - 20.)

Kikuma describes the construction of a device as in Figs. 9A, 9B as follows:

A semiconductor device 50 shown in FIG. 9A comprises four semiconductor chips 52-1 to 52-4 of the same type that are stacked and then connected to one another by wire bonding. This wire bonding process is performed first between the uppermost semiconductor chip 52-4 and the uppermost second substrate 32-3, and then performed between the uppermost second substrate 32-3 and the second substrate 32-2 immediately below the second substrate 32-3. In this manner, the wire bonding process is successively performed until the wire bonding between the lowermost second substrate 32-1 and the first substrate (the flexible printed wiring board 26). To perform collectively the wiring bonding process, each second substrate needs to be larger than the second substrate located immediately above, so as to prevent the bonding pads from being covered by the upper second substrate.

In a semiconductor device 60 shown in FIG. 9B, semiconductor chips 62-1 to 62-4 are stacked one by one, and the wire bonding process is performed for the each stacking process. More specifically, the lowermost semiconductor chip 62-1 is mounted on the first substrate (the flexible printed wiring board 26), and the lowermost second substrate 32-1 is then mounted on the lowermost semiconductor chip 62-1 by flip-chip bonding. At this point, a wire bonding process is performed between the second substrate 32-1 and the first substrate 26. Next, the second lowermost semiconductor chip 62-2 is secured onto the lowermost second substrate 32-1, and the second lowermost second substrate 32-2 is mounted on the semiconductor chip 62-2 by flip-chip bonding. A wire bonding process is then performed between the

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second lowermost second substrate 32-2 and the first substrate 26. In this manner, a wire bonding process is performed every time one second substrate is stacked on one semiconductor chip. When the uppermost semiconductor chip 62-4 is stacked on and connected to the uppermost second substrate 32-3 by wire bonding, all the wire bonding processes are completed. In this structure, all the second substrates can have the same size.

(Col. 11, lines 26 - 63; emphasis added herein.)

Thus, Kikuma expressly teaches building up a stacked semiconductor device by serially mounting semiconductor chips, and then (after the stack is complete) forming electrical connection of the chips by wire bonding. Kikuma does not teach stacking packages, or a module comprising stacked packages (nor a method for making such a multi-package module by stacking packages), as in Applicant's invention as claimed.

Rejections under 35 U.S.C. § 103(a)

Claim 5 was rejected under 35 U.S.C. § 103(a) for obviousness over Kikuma in view of Farnworth *et al.* U.S. 6,501,165 ("Farnworth"). Kikuma is applied as in the rejection of claim 1, and Farnworth is relied upon (with reference to Farnworth Fig. 4 and column 4, lines 11 and 12) as describing a second package substrate being a single-metal layer substrate (22).

Farnworth describes a stackable semiconductor package, and an electronic assembly constructed using multiple such packages. Farnworth expressly states regarding the package:

The package includes a substrate, and a semiconductor die attached to the substrate. The substrate comprises three separate layers including a conductive layer having conductive traces in a desired configuration, and first and second insulating layers on opposing sides of the conductive layer. One of the insulating layers covers the die, and one of the insulating layers covers the conductive traces. The package also includes electrically conductive vias through the insulating layers in electrical communication with the conductive traces. In addition, the package includes arrays of external contacts, such as pads or balls, arranged in matching patterns on each insulating layer in electrical communication with the conductive vias and the conductive traces.

(Col. 1, lines 53 - 65). And, regarding the assembly:

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Referring to FIG. 4, the electronic assembly 56 is illustrated. The assembly 56 comprises three separate packages 10-1, 10-2, 10-3 that have been stacked and bonded to one another. A solder reflow process, performed in an oven or with a localized heat source, can be used to bond the contact balls 54, and the external contacts 50, on adjacent packages 10. In addition, the contact balls 54 on the lowermost package 10-3 have been bonded to electrodes 72 on a supporting substrate 74 such as a printed circuit board or a multi chip module substrate. The construction of the packages 10-1, 10-2, 10-3 allows the contact balls 54 on the middle package 10-2 to be bonded to the external contacts 50 on the lowermost package 10-3. In addition, the contact balls 54 on the top package 10-1 are bonded to the external contacts 50 on the middle package 10-2.

(Col. 7, lines 5 - 17). The packages are connected by solder reflow of contact balls on a lower side of an upper package to external contacts on an upper side of a lower package. Nowhere in Farnworth is there any suggestion of first and second package substrates interconnected by wire bonding, as in Applicant's claimed invention.

As noted above, Kikuma fails to suggest or describe a multi-package module having stacked packages and, as there is no suggestion in Farnworth of first and second package substrates interconnected by wire bonding, Farnworth cannot supply what Farnworth lacks. Accordingly, no combination of Farnworth with Kikuma makes Applicant's claimed invention, and this rejection for obviousness should be withdrawn.

Claims 6 - 10, 13 and 19 were rejected under 35 U.S.C. § 103(a) for obviousness over Kikuma in view of Kakimoto *et al.* U.S. 6,333,552 ("Kakimoto"). Claims 14 - 16 were rejected under 35 U.S.C. § 103(a) for obviousness over Kikuma in View of Lin U.S. 5,436,203 ("Lin").

As to claims 6 - 10, 13 and 19, Kikuma is applied as in the rejection of claim 1, and Kakimoto is relied upon (with reference to Kakimoto Figs. 3 and 7) as describing an electrical shield and an RF die in a flip chip package. As noted above, Kikuma fails to suggest or describe a multi-package module having stacked packages and, as there is no suggestion in Kakimoto of stacked packages, Kakimoto cannot supply what Kikuma lacks. Accordingly, no combination of Kakimoto with Kikuma makes Applicant's claimed invention, and this rejection for obviousness should be withdrawn.

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As to claims 14 - 16, Kikuma is applied as in the rejection of claim 1, and Lin is relied upon (with reference to Lin Fig. 1) as describing an embedded ground plane in a package substrate. As noted above, Kikuma fails to suggest or describe a multi-package module having stacked packages and, as there is no suggestion in Lin of stacked packages, Lin cannot supply what Kikuma lacks. Accordingly, no combination of Lin with Kikuma makes Applicant's claimed invention, and this rejection for obviousness should be withdrawn.

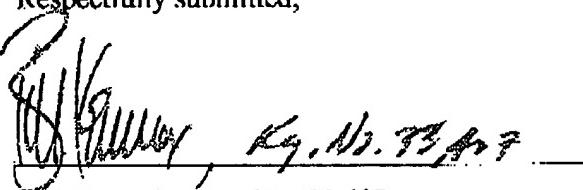
In view of the foregoing, all the claims now in the application are believed to be in condition for allowance, and action to that effect is respectfully requested.

If the Examiner believes a telephone conference would aid the prosecution of this case in any way, the Examiner is invited to telephone the undersigned at the number set out below.

This response is being made within the second month following the mailing of a Final Office action in the application and, accordingly, no extension of time or fee therefor is required in connection with the filing of this paper.

Respectfully submitted,

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